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Carrier Mobility Enhancement in Organic TFTs With Gate Insulator of Vertical Liquid Crystal Alignment Film

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In order to improve the carrier mobility of pentacene organic thin-film transistors (O-TFTs), we have studied the effect of the gate insulator material on the mobility. In spite of a reduction of the grain size, a gate insulating polymer material with a low surface energy, which is used for vertical alignment films for liquid crystals, significantly enhances the carrier mobility of the pentacene TFTs from ∼0.4 to up to ∼1.2 cm² Vs.

Keywords Pentacene; TFT; vertical alignment layer

1. Introduction

In the coming years, high-performance flexible liquid crystal displays (LCDs) using plastic substrates are expected to become a key device for next generation mobile displays. In such high-performance displays, active-matrix driving using thin-film transistors (TFTs) is essential, and significant effort has been made to fabricate TFTs on plastic substrates [1]. However, the fabrication of conventional inorganic (Si) TFTs needs rather high process temperatures of over 200°C, which is too high for handling conventional plastic substrates and thus impedes the realization of high-performance flexible displays. Replacement of inorganic TFTs with organic TFTs (O-TFTs) is one solution for overcoming such high process temperature problems for flexible displays using plastic substrates, and an increasing amount of research on organic TFTs has been conducted [2–4]. One important objective is to improve the carrier mobility, which is now almost comparable to that of a-Si TFTs [1]. In order to further improve the mobility, surface modification of the gate insulator with a self-assembled monolayer (SAM) has been proposed, and an improvement in the mobility was demonstrated [5,6]. A SAM is known to lower the surface energy of the gate insulator, which may improve the crystalline quality of an over-deposited organic semiconductor layer, and lead to an increase of the carrier mobility.

In this paper, we demonstrate that, by using a vertical liquid crystal (LC) alignment polymer film as the gate insulator, the carrier mobility of pentacene organic TFTs is drastically enhanced to over 1 cm^2 Vs.

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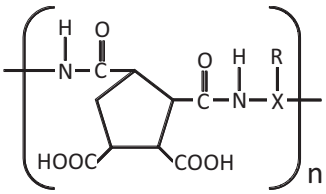

Figure 1. Chemical structure of JALS-204.

2. Experimental

A Ta_2O_5 gate-insulating layer, which is known to be a high-κ material [7], was deposited on patterned indium tin oxide (ITO)-coated glass substrates by a radio frequency (RF) magnetron sputtering method at room temperature (RT); the patterned ITO electrode was used as the gate electrode. During the deposition, mixture gases of argon and oxygen were introduced into the chamber with respective flow rates of 10 ccm and 3 ccm, which resulted in a background pressure of approximately 5.0×10^{-3} Torr. After depositing a Ta_2O_5 layer with a thickness of approximately 180 nm, an additional polymer gate-insulating layer of the vertical LC alignment polymer film (JALS-204 from JSR Corp.) was spin-coated on the Ta_2O_5 layer, yielding a double-stacked (DS) film. The polymer layer was then dried at 180°C for 1 h to remove the solvent in the film. This polymer material has alkyl branches that provide a low surface energy similar to the SAM films [8]. The chemical structure of the JALS-204 polymer is shown in Fig. 1, where R denotes an alkyl branch.

We used as-purchased pentacene as the deposition source for the organic semiconducting layer, which was thermally evaporated on a polymer gate-insulator layer under a background pressure of 1.0×10^{-7} to 5.0×10^{-8} Torr. Here, the substrate was kept at RT during the deposition, and the deposition rate and thickness of the pentacene layer were approximately 0.2 nm/s and 100 nm, respectively. Finally, Au source-drain electrodes were evaporated onto the pentacene semiconductor layer through a shadow mask, which defined the channel length and width as 50 μm and 1 mm, respectively. The overall structure of the fabricated O-TFT is shown in Fig. 2.

For evaluating the formation of the conduction channel at the insulator/semiconductor interface, capacitance-voltage (C-V) measurements (HP4284A) of metal-insulator-semiconductor (MIS) samples were conducted by varying a DC bias voltage with a small AC signal of 10 kHz, while, for the TFT characterizations, current-voltage (I-V) measurements were performed using the HP4140B pA meter. All measurements were conducted at RT under an air atmosphere.

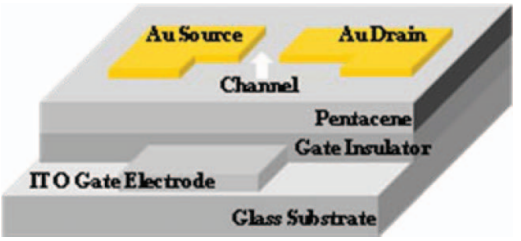

Figure 2. Schematic drawing of O-TFT structure.

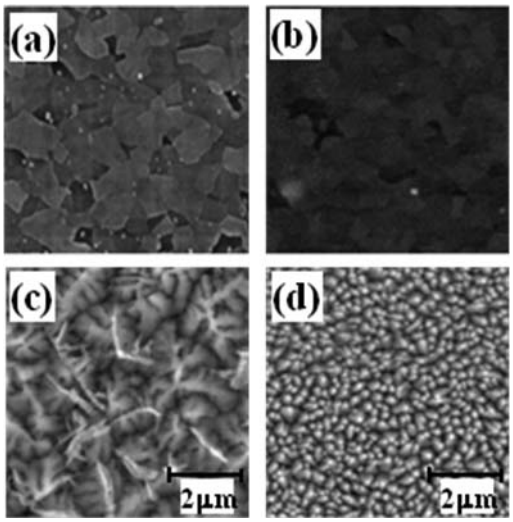

Figure 3. AFM images of (a) Ta_2O_5, (b) JALS-204 on Ta_2O_5, (c) pentacene on Ta_2O_5, and (d) pentacene on DS film.

3. Results and Discussion

As reported previously [5,6], surface modification of the gate insulator with a SAM film, which reduces the surface energy of the insulator, is known to enhance the carrier mobility of an overgrown organic semiconducting layer. This enhancement indicates an improvement of the crystalline quality of the organic semiconductor layer near the semiconductor/insulator interface (i.e., the conducting channel region).

First, we investigated the effect of the surface energy of the growth substrate on the growth mode of the pentacene layer. The surface morphology of thermally deposited pentacene on two types of substrate surfaces was observed by an atomic force microscope (AFM). Figure 3 displays AFM surface images of 100 nm-thick pentacene layers on Ta_2O_5 (Fig. 3(c)) and the DS film (Fig. 3(d)); the surface energy of Ta_2O_5 is $\sim$68 mJ m^{-2} and that of the DS film is $\sim$33 mJ m^{-2}. For reference, we also show AFM surface images of Ta_2O_5 and the DF film in Figs. 3(a) and (b), respectively. As reported in previous research using a SiO_2 gate insulator [9], pentacene with a dendritic structure and a grain size of few micrometers is formed on Ta_2O_5 (Fig. 3(c)), while a smaller granular structure with a grain size of about 0.2–0.3 μm is observed on the DS film. This drastic change in the surface morphology originates in the different surface energy between the Ta_2O_5 and DS film, which may also result in a different surface mobility of the pentacene molecules on the two surfaces. These results indicate that the carrier mobility of pentacene films deposited on the two surfaces may be largely different from each other.

Next, we also investigated the crystalline quality of pentacene films deposited on Ta_2O_5 and the DS film by X-ray diffraction (XRD) measurements under a $\theta/2\theta$ mode. Table 1 shows the measured monolayer spacing, normalized intensity (peak intensity divided by the background intensity), and full width at half maximum (FWHM) of the XRD peaks for these two pentacene films. From the table, it can be seen that a higher normalized intensity, larger monolayer spacing, and narrower FWHM are recorded for the pentance layer on Ta_2O_5 than for that on the DS film. Although the monolayer spacing and FWHM

Table 1. XRD measurement results

	Ta_2O_5	DS film
Normalized intensity	∼140	∼5
Layer spacing (nm)	1.54	1.53
FWHM (deg.)	0.11	0.12

of the XRD peaks of the films do not differ from each other significantly, the normalized diffraction intensity drastically decreased for the pentacene grown on the DS film. These results possibly indicate that a better quality pentacene crystal was deposited on Ta_2O_5 than on the DS film.

From the AFM and XRD measurement results, an O-TFT with a Ta_2O_5 gate insulator should be expected to provide a higher carrier mobility than that with a DS gate insulator. However, as we will show, using a DS gate insulator for pentacene TFTs drastically enhances the carrier mobility of the O-TFTs.

In order to confirm the formation of the conduction channel at the interface between the insulator (Ta_2O_5 or DS film) and the pentacene layer, two MIS diodes with Ta_2O_5 and DS film were prepared, and the C-V measurements of the samples were carried out as shown in Fig. 4; plot (a) is for the MIS diode with a Ta_2O_5 insulator, and (b) is the data for that with a DS insulator. The results show a strong DC bias voltage dependence, which is a typical high-frequency C-V characteristic for MIS diodes. Here, a negative gate bias voltage induces a high capacitance value, indicating hole accumulation at the pentacene/insulator interface and, thus, the formation of a p-type conducting channel at the interface [10]. The lower capacitance value for the MIS diode with a DS insulator than that for Ta_2O_5 is due to smaller dielectric constant ($\varepsilon_r \approx 4$) of the polymer film used in DS film (and also a thicker film thickness) than that of Ta_2O_5 ($\varepsilon_r \approx 20$). A shift of the C-V curve to a negative voltage for the DS film can be seen in comparison with the C-V curve for Ta_2O_5. We can consider several origins for this shift, such as ions in the insulator layer or trapped carriers at interface states, but the details are not yet clear.

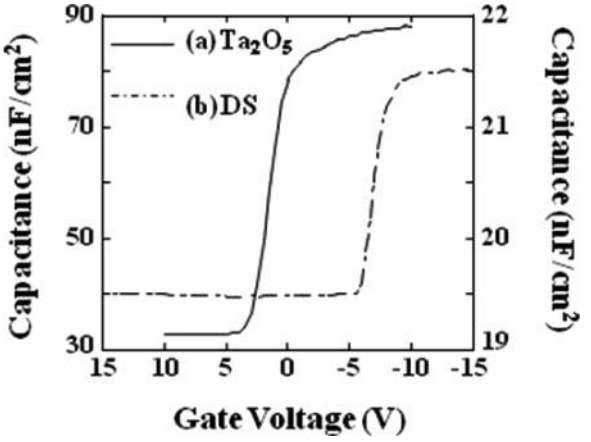

Figure 4. C-V characteristics of the MIS diodes with (a) Ta_2O_5 and (b) DS gate insulators.

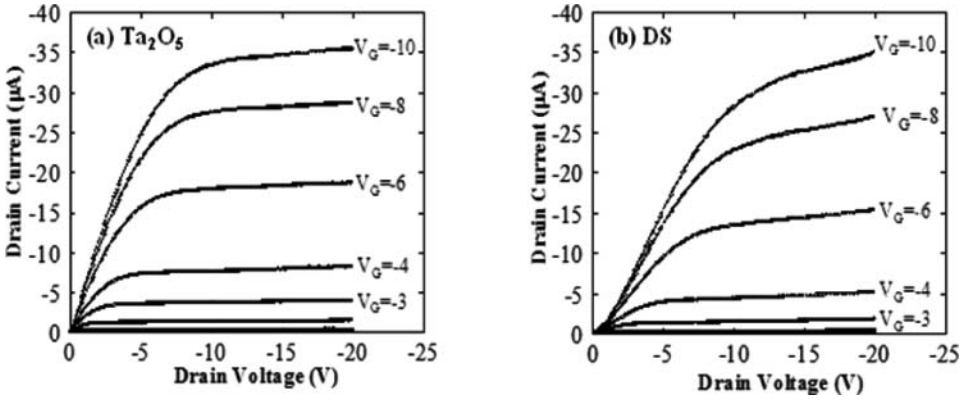

Figure 5. I_D-V_D characteristics of O-TFTs with (a) Ta_2O_5 and (b) DS gate insulators.

Figures 5(a) and (b) are the drain voltage (V_D) versus drain current (I_D) (V_D-I_D) characteristics as a function of the gate voltage (V_G) for an O-TFT with Ta_2O_5 and DS gate insulators, respectively. By comparing the I_D-V_D characteristics of the two samples, the maximum drain saturation current of an O-TFT with a DS gate insulator at a gate voltage of -10 V is almost comparable to that of an O-TFT with a Ta_2O_5 gate insulator. It should be noted that, in spite of the smaller capacitance value for the MIS diode with a DS gate insulator than that of the MIS diode with Ta_2O_5 as shown in Fig. 4, the maximum drain current for the two samples is almost the same at a gate voltage of -10 V. This indicates a higher carrier mobility in the O-TFT with a DS gate insulator.

From the results of the C-V (Fig. 4) and I_D-V_D characteristics for the two samples (Fig. 5), we can derive the hole carrier mobility (from a saturated region) and the I_{on}/I_{off} ratio of each sample. The results are shown in Table 2. Even for an O-TFT with a Ta_2O_5 gate insulator, a rather high hole carrier mobility of about 0.4 cm^2 Vs was obtained, which indicates rather high quality of the pentacene layer on Ta_2O_5. On the other hand, the hole carrier mobility for an O-TFT with a DS gate insulator drastically improves to about 1.2 cm^2 Vs, which exceeds the carrier mobility of conventional a-Si TFTs. Although the I_{on}/I_{off} ratios of the two samples are not high enough, one order of magnitude improvement in the I_{on}/I_{off} ratio is gained by using a DS gate insulator due to low leakage through the DS gate insulator.

The drastic improvement in the hole carrier mobility may indicate that the crystalline quality of a pentacene layer (interface) on a polymer film showing low surface free energy (DS film) is improved, which may result from (1) weak stress on the pentacene interface layer from the DS gate insulator showing low surface energy and (2) low interfacial states between the pentacene and DS film. We can say that the same carrier mobility enhancement

Table 2. Results of carrier mobility and I_{on}/I_{off} ratio

	O-TFT with Ta_2O_5	O-TFT with DS film
Carrier mobility (cm^2 Vs)	0.39 at $V_G = -10$	1.21 at $V_G = -10$
I_{on}/I_{off}	$7.4 \times 10_2$	$8.9 \times 10_3$

mechanism, as in the case for an O-TFT using a SAM film, may work for the presented sample.

4. Conclusion

We have shown that a pentacene layer on Ta_2O_5 film exhibited a dendritic surface structure with a grain size of few micrometers and a granular surface structure of the pentacene layer was observed on DS film with a reduced grain size of about 0.1 μm. In spite of the grain size reduction in O-TFTs with DS gate insulators, the hole carrier mobility of the O-TFTs was drastically enhanced from about 0.4 to up to 1.2 cm^2 Vs, which exceeds the carrier mobility of conventional a-Si TFTs. Throughout this study, we have demonstrated that a vertical LC alignment polymer film, which exhibits a low surface energy, was very effective for improving the carrier mobility of an O-TFT using a pentacene semiconducting layer.

References

[1] Dimitrakopoulos, C. D., & Mascaro, D. J. (2001). *IBM J. Res. Dev.*, *45*, 11.
[2] Fujisaki, Y., Inoue, Y., Kurita, T., Tokito, S., Fujikake, H., & Kikuchi, H. (2004). *Jpn. J. Appl. Phys.*, *43*, 372.
[3] Blanchet, G. B., Subramoney, S., Bailey, R. K., Jaycox, G. D., & Nuckolls, C. (2004). *Appl. Phys. Lett.*, *85*, 828.
[4] Kumar, A., & Whitesides, G. M. (1993). *Appl. Phys. Lett.*, *63*, 2002.
[5] Klauk, H., Halik, M., Zschieschang, U., Schmid, G., Radlik, W., & Weber, W. (2002). *J. Appl. Phys.*, *92*, 5259.
[6] Kelley, T. W., Boardman, L. D., Dunbar, T. D., Muyres, D. V., Pellerite, M. J., & Smith, T. P. (2003). *J. Phys. Chem. B*, *107*, 5877.
[7] Kouda, Y., Kobayashi, A., & Iimura, Y. (2004). In: *Proceedings of IDW '04*, p. 459. Niigata, Japan: ITE and SID.
[8] Houryu, H., Fukuba, Y., Kouda, Y., & Iimura, Y. (2006). In: *Proceedings of IDW '06*, p. 1691. Otsu, Japan: ITE and SID.
[9] Gundlach, D. J., Lin, Y. Y., Jackson, T. N., Nelson, S. F., & Schlom, D. G. (1997). *IEEE Electron Device Lett.*, *18*, 87.
[10] Sirringhous, H., Friend, R., Kawase, T., & Buergi, L. (2003). Chapter 9 in C.R. Kagan and P. Andry (Eds.) "Thin-Film Transistors." 427–473. New York: Marcel Dekker inc.